## CPU Supervisor

These devices combine three popular functions; Power-on Reset Control, Watchdog Timer and Supply Voltage Supervision. This combination lowers system cost, reduces board space requirements and increases reliability.

Applying power to the device activates the power-on reset circuit which holds $\overline{RESET}$/RESET active for a period of time. This allows the power supply and oscillator to stabilize before the processor can execute code.

The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time out interval, the device activates the $\overline{RESET}$/RESET signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.
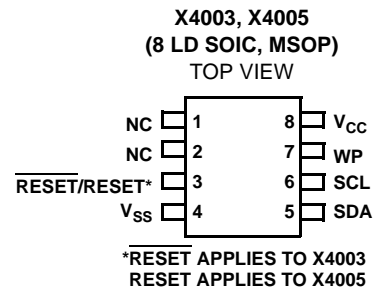
The device's low $V_{CC}$ detection circuitry protects the user's system from low voltage conditions, resetting the system when $V_{CC}$ falls below the minimum $V_{CC}$ trip point. $\overline{RESET}$/RESET is asserted until $V_{CC}$ returns to proper operating level and stabilizes. Five industry standard $V_{TRIP}$ thresholds are available; however, Intersil's unique circuits allow the threshold to be reprogrammed to meet custom requirements, or to fine-tune the threshold for applications requiring higher precision.
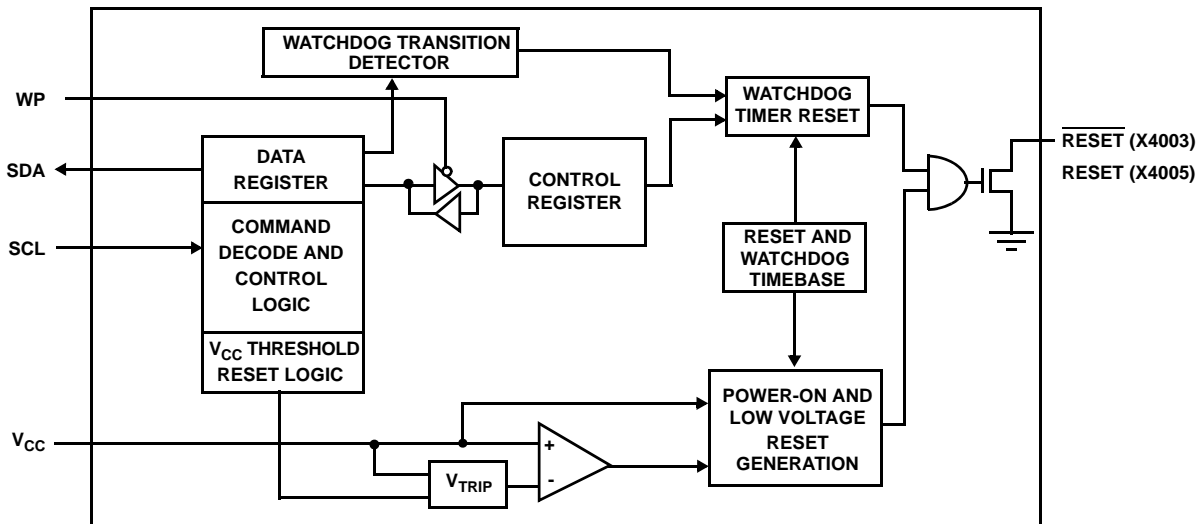
## Features

- Selectable watchdog timer
  - Select 200ms, 600ms, 1.4s, off
- Low $V_{CC}$ detection and reset assertion
  - Five standard reset threshold voltages nominal 4.62V, 4.38V, 2.92V, 2.68V, 1.75V
  - Adjust low $V_{CC}$ reset threshold voltage using special programming sequence
  - Reset signal valid to $V_{CC} = 1V$
- Low power CMOS
  - 12µA typical standby current, watchdog on
  - 800nA typical standby current watchdog off
  - 3mA active current
- 400kHz I²C interface
- 1.8V to 5.5V power supply operation
- Available packages
  - 8 Ld SOIC
  - 8 Ld MSOP
- Pb-free available (RoHS compliant)

## Pinout

**X4003, X4005**
**(8 LD SOIC, MSOP)**
TOP VIEW

```
         ┌────────┐
   NC  □ │1      8│ □ VCC
   NC  □ │2      7│ □ WP
RESET/  □ │3      6│ □ SCL
RESET*
   VSS □ │4      5│ □ SDA
         └────────┘
```

*$\overline{RESET}$ APPLIES TO X4003
RESET APPLIES TO X4005

## Block Diagram

## *Ordering Information*

| PART NUMBER RESET (ACTIVE LOW) | PART MARKING | PART NUMBER RESET (ACTIVE HIGH) | PART MARKING | $V_{CC}$ RANGE (V) | $V_{TRIP}$ RANGE (V) | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|---|---|---|---|---|
| X4003M8-4.5A | ACH | X4005M8-4.5A | ACQ | 4.5 to 5.5 | 4.5 to 4.75 | 0 to +70 | 8 Ld MSOP (3.0mm) | M8.118 |
| X4003M8Z-4.5A (Note) | DAH | X4005M8Z-4.5A (Note) | DAP | | | 0 to +70 | 8 Ld MSOP (3.0mm) (Pb-free) | M8.118 |
| X4003S8-4.5A | X4003 AL | X4005S8-4.5A | X4005 AL | | | 0 to +70 | 8 Ld SOIC (150 mil) | MDP0027 |
| X4003S8Z-4.5A (Note) | X4003 ZAL | X4005S8Z-4.5A (Note) | X4005 ZAL | | | 0 to +70 | 8 Ld SOIC (150 mil) (Pb-free) | MDP0027 |
| X4003M8I-4.5A | ACI | X4005M8I-4.5A | ACR | | | -40 to +85 | 8 Ld MSOP (3.0mm) | M8.118 |
| X4003M8IZ-4.5A (Note) | DAD | X4005M8IZ-4.5A (Note) | DAM | | | -40 to +85 | 8 Ld MSOP (3.0mm) (Pb-free) | M8.118 |
| X4003S8I-4.5A | X4003 AM | X4005S8I-4.5A | X4005 AM | | | -40 to +85 | 8 Ld SOIC (150 mil) | MDP0027 |
| X4003S8IZ-4.5A (Note) | X4003 ZAM | X4005S8IZ-4.5A (Note) | X4005 ZAM | | | -40 to +85 | 8 Ld SOIC (150 mil) (Pb-free) | MDP0027 |
| X4003M8 | ACJ | X4005M8 | ACS | | 4.25 to 4.5 | 0 to +70 | 8 Ld MSOP (3.0mm) | M8.118 |
| X4003M8Z (Note) | DAE | X4005M8Z (Note) | DER | | | 0 to +70 | 8 Ld MSOP (3.0mm) (Pb-free) | M8.118 |
| X4003S8 | X4003 | X4005S8 | X4005 | | | 0 to +70 | 8 Ld SOIC (150 mil) | MDP0027 |
| X4003S8Z (Note) | X4003 Z | X4005S8Z (Note) | X4005 Z | | | 0 to +70 | 8 Ld SOIC (150 mil) (Pb-free) | MDP0027 |
| X4003M8I | ACK | X4005M8I | ACT | | | -40 to +85 | 8 Ld MSOP (3.0mm) | M8.118 |
| X4003M8IZ (Note) | DAA | X4005M8IZ (Note) | DAJ | | | -40 to +85 | 8 Ld MSOP (3.0mm) (Pb-free) | M8.118 |
| X4003S8I | X4003 I | X4005S8I | X4005 I | | | -40 to +85 | 8 Ld SOIC (150 mil) | MDP0027 |
| X4003S8IZ (Note) | X4003 ZI | X4005S8IZ (Note) | X4005 ZI | | | -40 to +85 | 8 Ld SOIC (150 mil) (Pb-free) | MDP0027 |
| X4003M8-2.7A | ACL | X4005M8-2.7A | ACU | 2.7 to 5.5 | 2.85 to 3.0 | 0 to +70 | 8 Ld MSOP (3.0mm) | M8.118 |
| X4003M8Z-2.7A (Note) | DAG | X4005M8Z-2.7A (Note) | DAO | | | 0 to +70 | 8 Ld MSOP (3.0mm) (Pb-free) | M8.118 |
| X4003S8-2.7A | X4003 AN | X4005S8-2.7A | X4005 AN | | | 0 to +70 | 8 Ld SOIC (150 mil) | MDP0027 |
| X4003S8Z-2.7A (Note) | X4003 ZAN | X4005S8Z-2.7A (Note) | X4005 ZAN | | | 0 to +70 | 8 Ld SOIC (150 mil) (Pb-free) | MDP0027 |
| X4003M8-2.7 | ACN | X4005M8-2.7 | ACW | | 2.55 to 2.7 | 0 to +70 | 8 Ld MSOP (3.0mm) | M8.118 |
| X4003M8Z-2.7 (Note) | DAF | X4005M8Z-2.7 (Note) | DAN | | | 0 to +70 | 8 Ld MSOP (3.0mm) (Pb-free) | M8.118 |
| X4003S8-2.7 | X4003 F | X4005S8-2.7 | X4005 F | | | 0 to +70 | 8 Ld SOIC (150 mil) | MDP0027 |
| X4003S8Z-2.7 (Note) | X4003 ZF | X4005S8Z-2.7 | X4005 ZF | | | 0 to +70 | 8 Ld SOIC (150 mil) (Pb-free) | MDP0027 |

## Ordering Information (Continued)

| PART NUMBER RESET (ACTIVE LOW) | PART MARKING | PART NUMBER RESET (ACTIVE HIGH) | PART MARKING | V_CC RANGE (V) | V_TRIP RANGE (V) | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|---|---|---|---|---|
| X4003S8I-2.7A | X4003 AP | X4005S8I-2.7A | X4005 AP | 2.7 to 3.6 | 2.85 to 3.0 | -40 to +85 | 8 Ld SOIC (150 mil) | MDP0027 |
| X4003S8IZ-2.7A (Note) | X4003 ZAP | X4005S8IZ-2.7A (Note) | X4005 ZAP | | | -40 to +85 | 8 Ld SOIC (150 mil) (Pb-free) | MDP0027 |
| X4003M8I-2.7A | ACM | X4005M8I-2.7A | ACV | | | -40 to +85 | 8 Ld MSOP (3.0mm) | M8.118 |
| X4003M8IZ-2.7A (Note) | DAC | X4005M8IZ-2.7A (Note) | DAL | | | -40 to +85 | 8 Ld MSOP (3.0mm) (Pb-free) | M8.118 |
| X4003S8I-2.7 | X4003 G | X4005S8I-2.7 | X4005 G | | 2.55 to 2.7 | -40 to +85 | 8 Ld SOIC (150 mil) | MDP0027 |
| X4003S8IZ-2.7 (Note) | X4003 ZG | X4005S8IZ-2.7 (Note) | X4005 ZG | | | -40 to +85 | 8 Ld SOIC (150 mil) (Pb-free) | MDP0027 |
| X4003M8I-2.7 | ACO | X4005M8I-2.7 | ACX | | | -40 to +85 | 8 Ld MSOP (3.0mm) | M8.118 |
| X4003M8IZ-2.7 (Note) | DAB | X4005M8IZ-2.7 (Note) | DAK | | | -40 to +85 | 8 Ld MSOP (3.0mm) (Pb-free) | M8.118 |

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Pin Descriptions

| PIN NUMBER (MSOP) | NAME | FUNCTION |
|---|---|---|
| 1 | NC | No internal connections |
| 2 | NC | No internal connections |
| 3 | $\overline{RESET}$/RESET | **Reset Output.** $\overline{RESET}$/RESET is an active LOW/HIGH, open drain output which goes active whenever $V_{CC}$ falls below the minimum $V_{CC}$ sense level. It will remain active until $V_{CC}$ rises above the minimum $V_{CC}$ sense level for 250ms. $\overline{RESET}$/RESET goes active if the watchdog timer is enabled and SDA remains either HIGH or LOW longer than the selectable Watchdog time out period. A falling edge of SDA, while SCL also toggles from HIGH to LOW followed by a stop condition resets the watchdog timer. $\overline{RESET}$/RESET goes active on power-up and remains active for 250ms after the power supply stabilizes. |
| 4 | $V_{SS}$ | Ground |
| 5 | SDA | **Serial Data.** SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. This pin requires a pull-up resistor and the input buffer is always active (not gated). **Watchdog Input.** A HIGH to LOW transition on the SDA while SCL also toggles from HIGH to LOW follow by a stop condition resets the watchdog timer. The absence of this procedure within the watchdog time-out period results in $\overline{RESET}$/RESET going active. |
| 6 | SCL | **Serial Clock.** The serial clock controls the serial bus timing for data input and output. |
| 7 | WP | **Write Protect.** WP HIGH prevents changes to the watchdog timer setting. |
| 8 | $V_{CC}$ | Supply voltage |

## Principles of Operation

### Power-on Reset

Application of power to the X4003/X4005 activates a power-on reset circuit that pulls the $\overline{RESET}$/RESET pin active. This signal provides several benefits:

- It prevents the system microprocessor from starting to operate with insufficient voltage.

- It prevents the processor from operating prior to stabilization of the oscillator.

- It allows time for an FPGA to download its configuration prior to initialization of the circuit.

When $V_{CC}$ exceeds the device $V_{TRIP}$ threshold value for 200ms (nominal) the circuit releases $\overline{RESET}$/RESET, allowing the system to begin operation.

### Low Voltage Monitoring

During operation, the X4003/X4005 monitors the $V_{CC}$ level and asserts $\overline{RESET}$/RESET if supply voltage falls below a preset minimum $V_{TRIP}$. The $\overline{RESET}$/RESET signal prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{RESET}$/RESET signal remains active until the voltage drops below 1V. It also remains active until $V_{CC}$ returns and exceeds $V_{TRIP}$ for 200ms.

### Watchdog Timer

The watchdog timer circuit monitors the microprocessor activity by monitoring the SDA and SCL pins. The microprocessor must toggle the SDA pin HIGH to LOW periodically, while SCL also toggles from HIGH to LOW (this is a start bit) followed by a stop condition prior to the expiration of the watchdog time-out period to prevent a $\overline{RESET}$/RESET signal. The state of two nonvolatile control bits in the control register determine the watchdog timer period. The microprocessor can change these watchdog bits, or they may be "locked" by tying the WP pin HIGH.
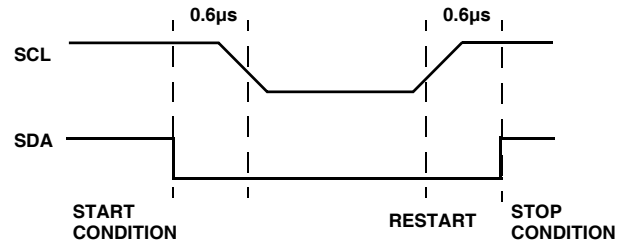


**FIGURE 1. WATCHDOG RESTART**

## $V_{CC}$ Threshold Reset Procedure

The X4003/X4005 is shipped with a standard $V_{CC}$ threshold ($V_{TRIP}$) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard $V_{TRIP}$ is not exactly right, or if higher precision is needed in the $V_{TRIP}$ value, the X4003/X4005 threshold may be adjusted. The procedure is described in the following and uses the application of a nonvolatile control signal.

### Setting the $V_{TRIP}$ Voltage

This procedure is used to set the $V_{TRIP}$ to a higher voltage value. For example, if the current $V_{TRIP}$ is 4.4V and the new $V_{TRIP}$ is 4.6V, this procedure will directly make the change. If the new setting is to be lower than the current setting, then it is necessary to reset the trip point before setting the new value.

To set the new $V_{TRIP}$ voltage, apply the desired $V_{TRIP}$ threshold voltage to the $V_{CC}$ pin and tie the WP pin to the programming voltage $V_P$. Then write data 00h to address 01h. The stop bit following a valid write operation initiates the $V_{TRIP}$ programing sequence. Bring WP LOW to complete the operation.
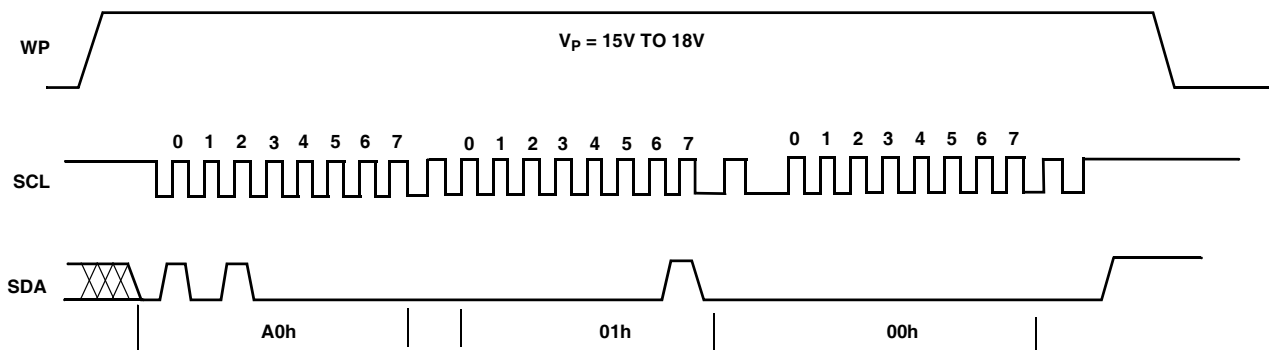


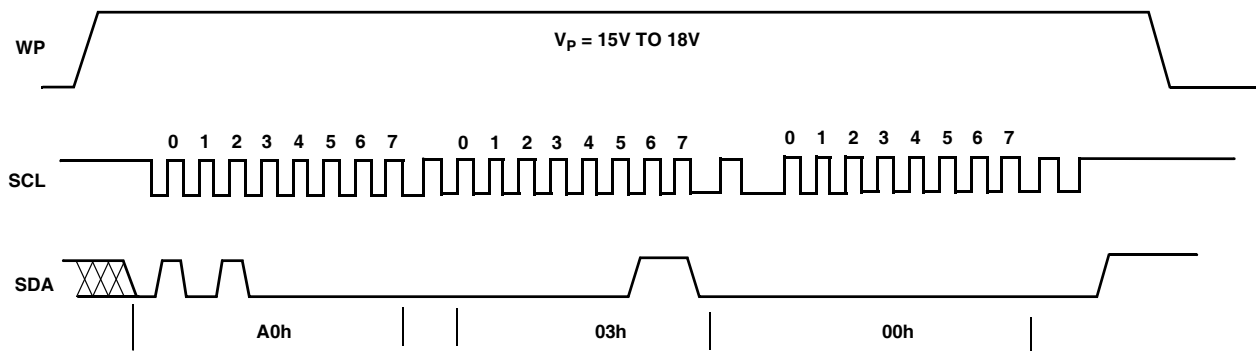**FIGURE 2. SET V_{TRIP} LEVEL SEQUENCE (V_{CC} = DESIRED V_{TRIP} VALUE)**

**FIGURE 3. RESET $V_{TRIP}$ LEVEL SEQUENCE ($V_{CC}$ > 3V. $\overline{WP}$ = 15V TO 18V)**
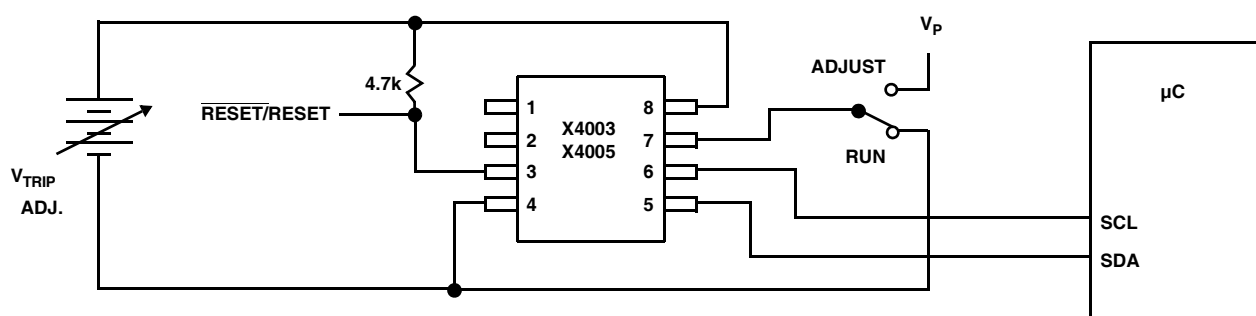


**FIGURE 4. SAMPLE $V_{TRIP}$ RESET CIRCUIT**

### *Resetting the $V_{TRIP}$ Voltage*

This procedure is used to set the $V_{TRIP}$ to a "native" voltage level. For example, if the current $V_{TRIP}$ is 4.4V and the new $V_{TRIP}$ must be 4.0V, then the $V_{TRIP}$ must be reset. When $V_{TRIP}$ is reset, the new $V_{TRIP}$ is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the new $V_{TRIP}$ voltage, apply the desired $V_{TRIP}$ threshold voltage to the $V_{CC}$ pin and tie the WP pin to the programming voltage $V_P$. Then write 00h to address 03h. The stop bit of a valid write operation initiates the $V_{TRIP}$ programming sequence. Bring WP LOW to complete the operation.
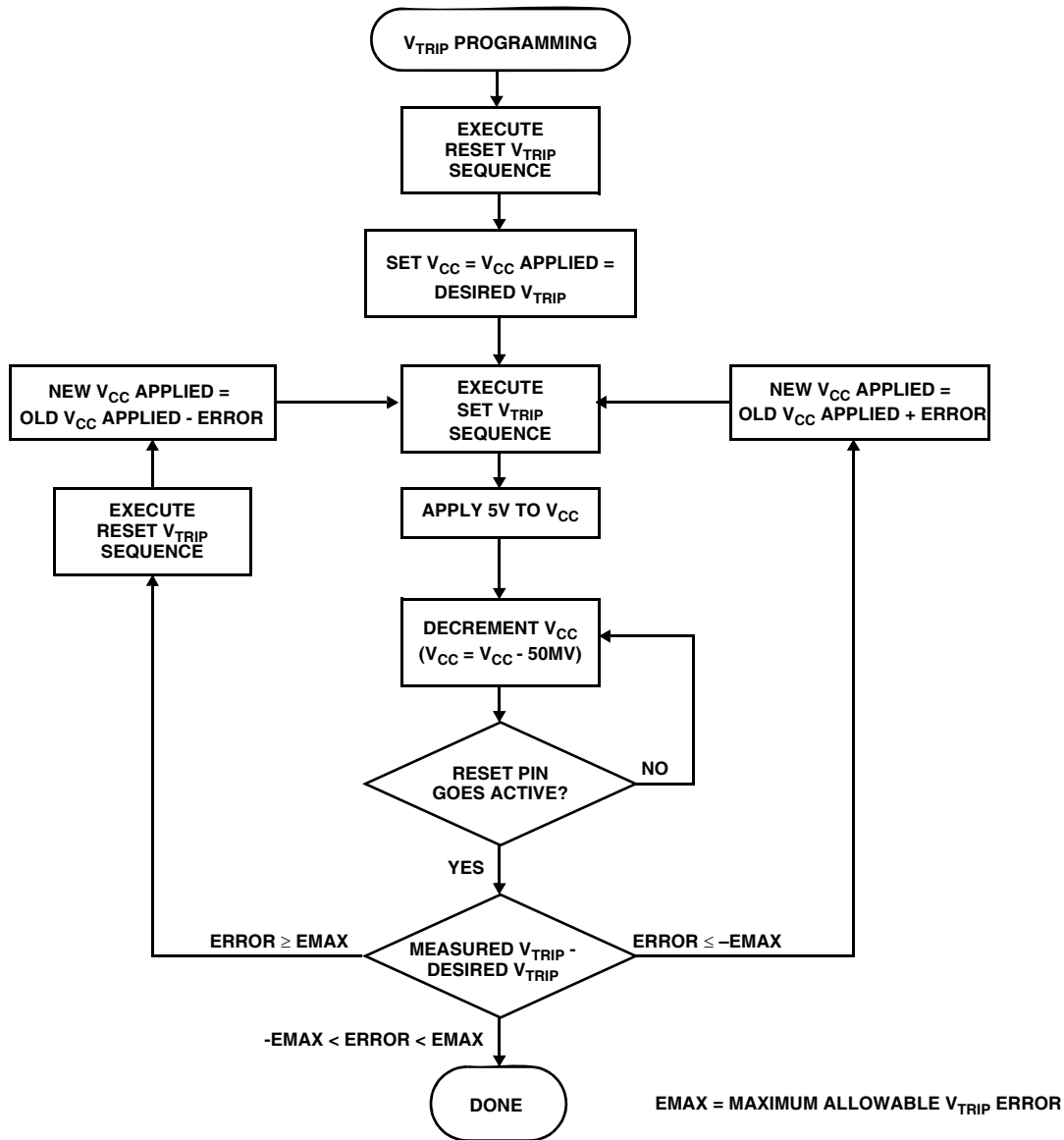
**FIGURE 5. V<sub>TRIP</sub> PROGRAMMING SEQUENCE**

### Control Register

The control register provides the user a mechanism for changing the watchdog timer settings. Watchdog timer bits are nonvolatile and do not change when power is removed.

The control register is accessed with a special preamble in the slave byte (1011) and is located at address 1FFh. It can only be modified by performing a control register write operation. Only one data byte is allowed for each register write operation. Prior to writing to the control register, the WEL and RWEL bits must be set using a two step process, with the whole sequence requiring 3 steps. See "Writing to the Control Register" on page 7.

The user must issue a stop after sending the control byte to the register to initiate the nonvolatile cycle that stores WD1

and WD0. The X4003/X4005 will not acknowledge any data bytes written after the first byte is entered.

The state of the control register can be read at any time by performing a serial read operation. Only one byte is read by each register read operation. The X4003/X4005 resets itself after the first byte is read. The master should supply a stop condition to be consistent with the bus protocol, but a stop is not required to end this operation.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | WD1 | WD0 | 0 | 0 | RWEL | WEL | 0 |

### RWEL: Register Write Enable Latch (Volatile)

The RWEL bit must be set to "1" prior to a write to the control register.

### WEL: Write Enable Latch (Volatile)

The WEL bit controls the access to the control register during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes the control register will be ignored (no acknowledge will be issued after the data byte). The WEL bit is set by writing a "1" to the WEL bit and zeroes to the other bits of the control register. Once set, WEL remains set until either it is reset to 0 (by writing a "0" to the WEL bit and zeroes to the other bits of the control register) or until the part powers up again. Writes to the WEL bit do not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition.

### WD1, WD0: Watchdog Timer Bits

The bits WD1 and WD0 control the period of the watchdog timer. The options are shown in the following:

| WD1 | WD0 | WATCHDOG TIME-OUT PERIOD |
|-----|-----|--------------------------|
| 0 | 0 | 1.4s |
| 0 | 1 | 600ms |
| 1 | 0 | 200ms |
| 1 | 1 | Disabled (factory setting) |

### Writing to the Control Register

Changing any of the nonvolatile bits of the control register requires the following steps:

- Write a 02H to the control register to set the write enable latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceeded by a start and ended with a stop.)

- Write a 06H to the control register to set both the register write enable latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation preceeded by a start and ended with a stop.)

- Write a value to the control register that has all the control bits set to the desired state. This can be represented as

0xy0 0010 in binary, where xy are the WD bits. (Operation preceeded by a start and ended with a stop.) Since this is a nonvolatile write cycle it will take up to 10ms to complete. The RWEL bit is reset by this cycle and the sequence must be repeated to change the nonvolatile bits again. If bit 2 is set to '1' in this third step (0xy0 0110) then the RWEL bit is set, but the WD1 and WD0 bits remain unchanged. Writing a second byte to the control register is not allowed. Doing so aborts the write operation and returns a NACK.

- A read operation occurring between any of the previous operations will not interrupt the register write operation.

- The RWEL bit cannot be reset without writing to the nonvolatile control bits in the control register, power cycling the device or attempting a write to a write protected block.

To illustrate, a sequence of writes to the device consisting of [02H, 06H, 02H] will reset all of the nonvolatile bits in the control register to 0. A sequence of [02H, 06H, 06H] will leave the nonvolatile bits unchanged and the RWEL bit remains set.

## Serial Interface

### Serial Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

### Serial Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 6.
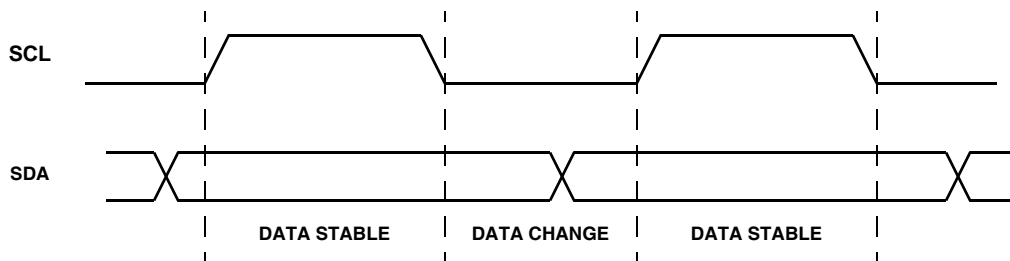


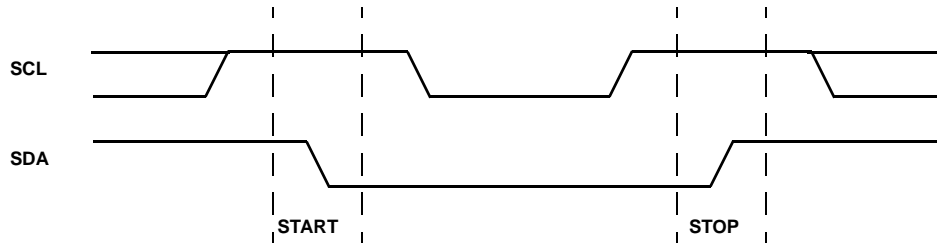**FIGURE 6. VALID DATA CHANGES ON THE SDA BUS**
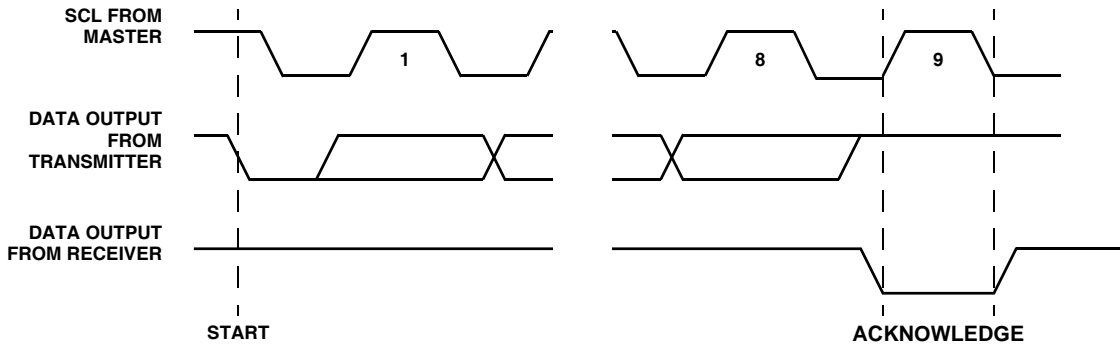
FIGURE 7.  VALID START AND STOP CONDITIONS



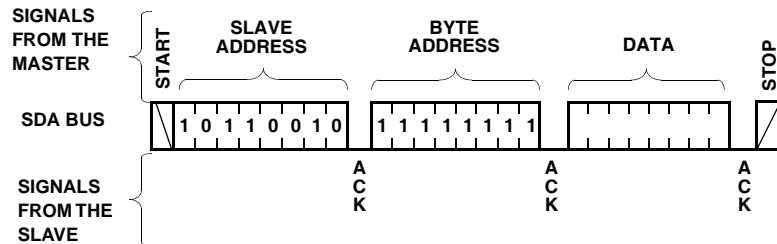FIGURE 8.  ACKNOWLEDGE RESPONSE FROM RECEIVER



FIGURE 9.  WRITE CONTROL REGISTER SEQUENCE

### *Serial Start Condition*

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 7.

### *Serial Stop Condition*

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. See Figure 7.

### *Serial Acknowledge*

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 8.

The device will respond with an acknowledge after recognition of a start condition and the correct contents of the slave address byte. Acknowledge bits are also provided by the X4003/4005 after correct reception of the control register address byte, after receiving the byte written to the control register and after the second slave address in a read question (see Figures 9 and 10).

## *Serial Write Operations*

### *Slave Address Byte*

Following a start condition, the master must output a slave address byte. This byte consists of several parts:

• a device type identifier that is always '1011'.

• two bits of '0'.

• one bit of the slave command byte is a R/$\overline{W}$ bit. The R/$\overline{W}$ bit of the slave address byte defines the operation to be

performed. When the R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation. Refer to Figure 9.

- After loading the entire slave address byte from the SDA bus, the device compares the input slave byte data to the proper slave byte. Upon a correct compare, the device outputs an acknowledge on the SDA line.

### Write Control Register

To write to the control register, the device requires the slave address byte and a byte address. This gives the master access to register. After receipt of the address byte, the device responds with an acknowledge, and awaits the data. After receiving the 8 bits of the data byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. During this internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. If WP is HIGH, the control register cannot be changed. A write to the control register will suppress the acknowledge bit and no data in the control register will change. With WP low, a second byte written to the control register terminates the operation and no write occurs.

### Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending 1 full data byte plus the subsequent ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte plus its associated ACK is sent, then the device will reset itself without performing the write.

### Serial Read Operations

The read operation allows the master to access the control register. To conform to the I²C standard, prior to issuing the slave address byte with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition and the slave address byte, receives an acknowledge, then issues the byte address. After acknowledging receipt of the byte address, the master immediately issues another start condition and the slave address byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit control register. The master terminates the read operation by not responding with an acknowledge and then issuing a stop

condition. Refer to Figure 10 for the address, acknowledge, and data transfer sequences.

### Operational Notes

The device powers-up in the following state:

- The device is in the low power standby state.

- The WEL bit is set to '0'. In this state it is not possible to write to the device.

- SDA pin is the input mode.

$\overline{RESET}$/RESET signal is active for $t_{PURST}$.

### Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The WEL bit must be set to allow a write operation.

- The proper clock count and bit sequence is required prior to the stop bit in order to start a nonvolatile write cycle.

- A three step sequence is required before writing into the control register to change watchdog timer or block lock settings.

- The WP pin, when held HIGH, prevents all writes to the control register.

- Communication to the device is inhibited below the $V_{TRIP}$ voltage.

- Command to change the control register are terminated if in-progress when $\overline{RESET}$/RESET go active.

### Symbol Table

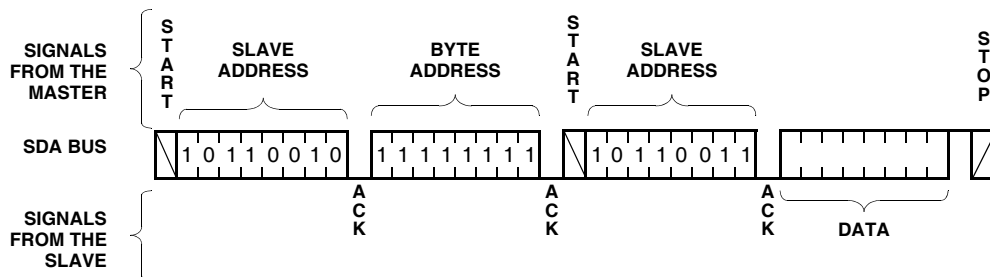| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from LOW to HIGH | Will change from LOW to HIGH |
| | May change from HIGH to LOW | Will change from HIGH to LOW |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |



**FIGURE 10. CONTROL REGISTER READ SEQUENCE**

## Absolute Maximum Ratings

Temperature Under Bias . . . . . . . . . . . . . . . . . . . . . .-65°C to +135°C
Voltage on any Pin with Respect to $V_{SS}$ . . . . . . . . . . . .-1.0V to +7V
DC Output Current. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5mA

## Operating Conditions

Temperature Range. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
  Commerical . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0°C to +70°C
  Industrial. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .-40°C to +85°C

## Thermal Information

Maximum Storage Temperature Range. . . . . . . . . . .-65°C to +150°C
Pb-free reflow profile . . . . . . . . . . . . . . . . . . . . . . . . . .see link below
  http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## DC Operating Characteristics
Over the recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $V_{CC}$ = 1.8 TO 3.6V | | $V_{CC}$ = 2.7 TO 5.5V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $I_{CC}$ (Note 1) | Active Supply Current Read Control Register | $f_{SCL}$ = 400kHz nonvolatile, SDA = Open | | 0.5 | | 1.0 | mA |
| $I_{CC2}$ (Note 1) | Active Supply Current Write Control Register | $f_{SCL}$ = 400kHz nonvolatile, SDA = Open | | 1.5 | | 3.0 | mA |
| $I_{CC3}$ (Note 2) | Operating Current AC (WDT Off) | $f_{SCL}$ = 400kHz nonvolatile, SDA = Open | | 1 | | 1 | µA |
| $I_{CC4}$ (Note 2) | Operating Current DC (WDT Off) | $V_{SDA} = V_{SCL} = V_{CC}$ Others = GND or $V_{SB}$ | | 1 | | 1 | µA |
| $I_{CC5}$ (Note 2) | Operating Current DC (WDT On) | $V_{SDA} = V_{SCL} = V_{CC}$ Others = GND or $V_{SB}$ | | 10 | | 20 | µA |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = GND to $V_{CC}$ | | 10 | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{SDA}$ = GND to $V_{CC}$ Device is in Standby (Note 2) | | 10 | | 10 | µA |
| $V_{IL}$ (Note 3) | Input LOW Voltage | | -0.5 | $V_{CC}$ x 0.3 | -0.5 | $V_{CC}$ x 0.3 | V |
| $V_{IH}$ (Note 3) | Input HIGH Voltage | | $V_{CC}$ x 0.7 | $V_{CC}$ + 0.5 | $V_{CC}$ x 0.7 | $V_{CC}$ + 0.5 | V |
| $V_{HYS}$ | Schmitt Trigger Input Hysteresis | | | | | | |
| |     Fixed Input Level | | 0.2 | | 0.2 | | V |
| |     $V_{CC}$ Related Level | | 0.05 x $V_{CC}$ | | 0.05 x $V_{CC}$ | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 3.0mA (2.7V to 5.5V) $I_{OL}$ = 1.8mA (1.8V to 3.6V) | | 0.4 | | 0.4 | V |

NOTES:

1. The device enters the active state after any start, and remains active until: 9 clock cycles later if the device select bits in the slave address byte are incorrect; 200ns after a stop ending a read operation; or $t_{WC}$ after a stop ending a write operation.

2. The device goes into standby: 200ns after any stop, except those that initiate a nonvolatile write cycle; $t_{WC}$ after a stop that initiates a nonvolatile cycle; or 9 clock cycles after any start that is not followed by the correct device select bits in the slave address byte.

3. $V_{IL}$ min. and $V_{IH}$ max. are for reference only and are not tested.

## Capacitance
($T_A$ = +25°C, f = 1.0 MHz, $V_{CC}$ = 5V)

| SYMBOL | PARAMETER | TYP | UNIT | TEST CONDITIONS |
|---|---|---|---|---|
| $C_{OUT}$ | Output Capacitance (SDA, $\overline{\text{RESET}}$/RESET) | 8 | pF | $V_{OUT}$ = 0V |
| $C_{IN}$ | Input Capacitance (SCL, WP) | 6 | pF | $V_{IN}$ = 0V |

## Equivalent AC Load Circuit
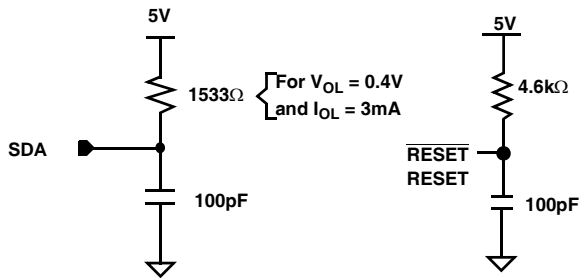


## AC Test Conditions

| Input pulse levels | $0.1V_{CC}$ to $0.9V_{CC}$ |
|---|---|
| Input rise and fall times | 10ns |
| Input and output timing levels | $0.5V_{CC}$ |
| Output load | Standard output load |

## AC Electrical Specifications
Over recommended operating conditions, unless otherwise specified.

| SYMBOL | PARAMETER | 100kHz | | 400kHz | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $f_{SCL}$ | SCL Clock Frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{IN}$ | Pulse Width Suppression Time at Inputs | n/a | n/a | 50 | | ns |
| $t_{AA}$ | SCL LOW to SDA Data Out Valid | 0.1 | 0.9 | 0.1 | 0.9 | µs |
| $t_{BUF}$ | Time the Bus Free Before Start of New Transmission | 4.7 | | 1.3 | | µs |
| $t_{LOW}$ | Clock LOW Time | 4.7 | | 1.3 | | µs |
| $t_{HIGH}$ | Clock HIGH Time | 4.0 | | 0.6 | | µs |
| $t_{SU:STA}$ | Start Condition Set-up Time | 4.7 | | 0.6 | | µs |
| $t_{HD:STA}$ | Start Condition Hold Time | 4.0 | | 0.6 | | µs |
| $t_{SU:DAT}$ | Data in Setup Time | 250 | | 100 | | ns |
| $t_{HD:DAT}$ | Data in Hold Time | 5.0 | | 0 | | µs |
| $t_{SU:STO}$ | Stop Condition Set-up Time | 0.6 | | 0.6 | | µs |
| $t_{DH}$ | Data Output Hold Time | 50 | | 50 | | ns |
| $t_R$ | SDA and SCL Rise Time | | 1000 | 20 + 0.1Cb (Note 5) | 300 | ns |
| $t_F$ | SDA and SCL Fall Time | | 300 | 20 + 0.1Cb (Note 5) | 300 | ns |
| $t_{SU:WP}$ | $\overline{WP}$ Set-up Time | 0.4 | | 0.6 | | µs |
| $t_{HD:WP}$ | $\overline{WP}$ Hold Time | 0 | | 0 | | µs |
| Cb | Capacitive Load for Each Bus Line | | 400 | | 400 | pF |

NOTES:

4. Typical values are for $T_A$ = +25°C and $V_{CC}$ = 5.0V

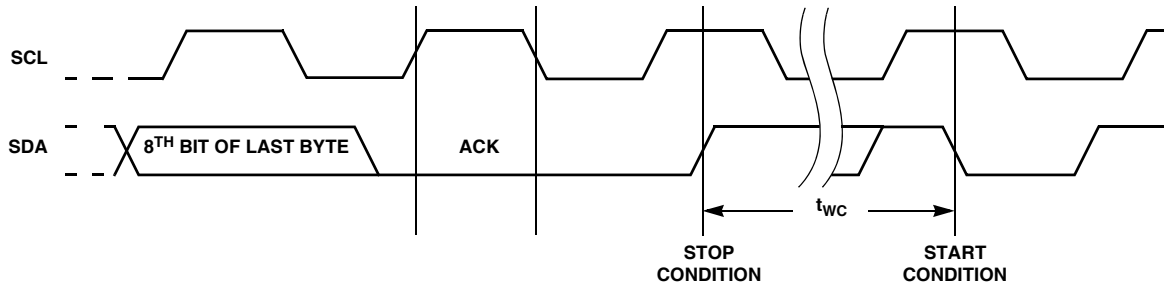5. Cb = total capacitance of one bus line in pF

# Timing Diagrams

## Bus Timing
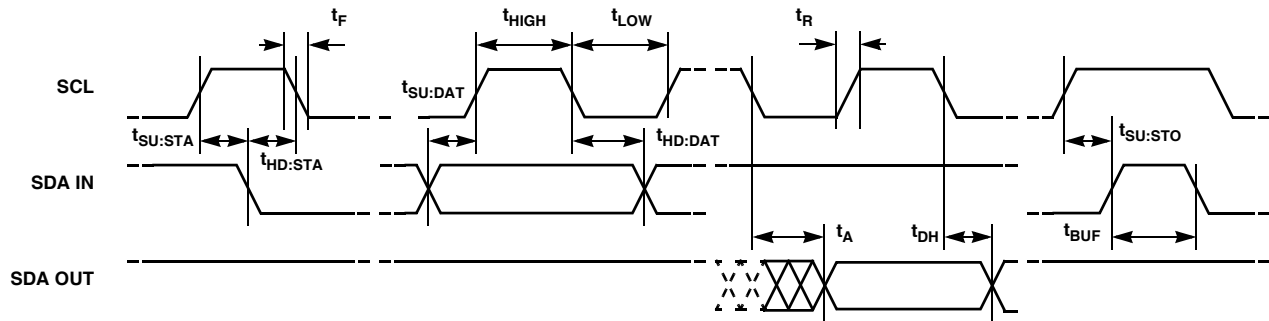


## WP Pin Timing
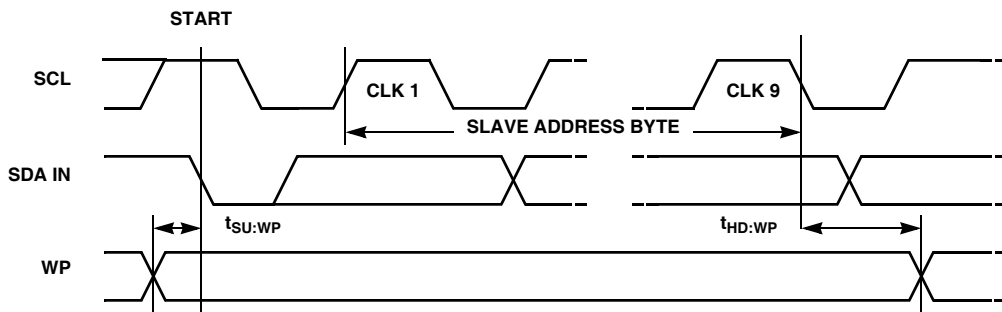


## Write Cycle Timing



### Nonvolatile Write Cycle Timing

| SYMBOL | PARAMETER | MIN | TYP (Note 1) | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{WC}$ (Note 6) | Write Cycle Time | | 5 | 10 | ms |

NOTE:

6. $t_{WC}$ is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.
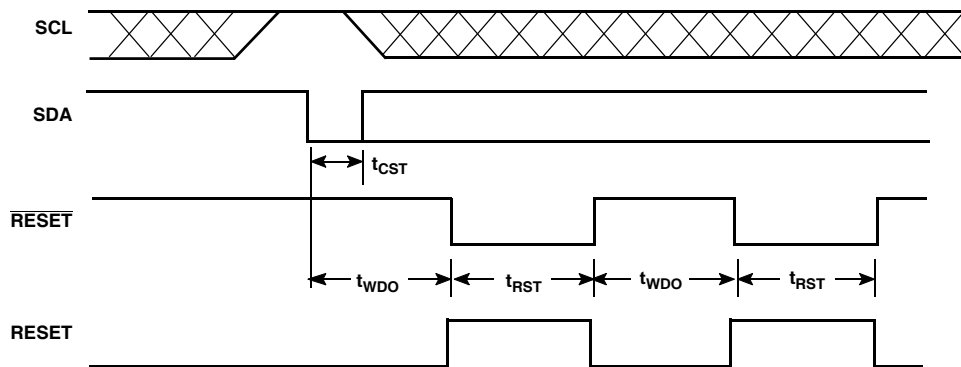
### *Power-Up and Power-Down Timing*
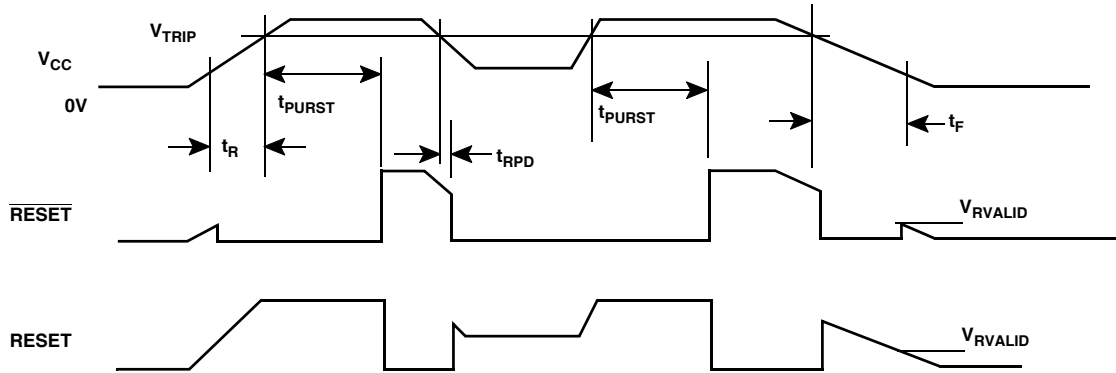


### $\overline{RESET}$/RESET Output Timing

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|--------|-----------|-----|-----|-----|------|
| $V_{TRIP}$ | Reset Trip Point Voltage, X4003-4.5A, X4005-4.5A | 4.5 | 4.62 | 4.75 | V |
| | Reset Trip Point Voltage, X4003, X4005 | 4.25 | 4.38 | 4.5 | V |
| | Reset Trip Point Voltage, X4003-2.7A, X4005-2.7A | 2.85 | 2.92 | 3.0 | V |
| | Reset Trip Point Voltage, X4003-2.7, X4005-2.7 | 2.55 | 2.62 | 2.7 | V |
| | Reset Trip Point Voltage, X4003-1.8, X4005-1.8 | 1.7 | 1.75 | 1.8 | V |
| $t_{PURST}$ | Power-up Reset Time-out | 100 | 200 | 400 | ms |
| $t_{RPD}$ | $V_{CC}$ Detect to Reset Output | | 500 | | ns |
| $t_F$ | $V_{CC}$ Fall Time | | 10 | | ms |
| $t_R$ | $V_{CC}$ Rise Time | | 0.1 | | ns |
| $V_{RVALID}$ | Reset Valid $V_{CC}$ | 1 | | | V |

### *SDA vs RESET/RESET Timing*



### RESET/RESET Output Timing

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|--------|-----------|-----|-----|-----|------|
| $t_{WDO}$ | Watchdog Time-out Period | | | | |
| | WD1 = 1, WD0 = 1 (factory setting) | | OFF | | |
| | WD1 = 1, WD0 = 0 | 100 | 200 | 300 | ms |
| | WD1 = 0, WD0 = 1 | 450 | 600 | 800 | ms |
| | WD1 = 0, WD0 = 0 | 1 | 1.4 | 2 | sec |
| $t_{CST}$ | $\overline{CS}$ Pulse Width to Reset the Watchdog | 400 | | | ns |
| $t_{RST}$ | Reset Time-out | 100 | 200 | 400 | ms |

## *V<sub>TRIP</sub> Programming Timing Diagram*
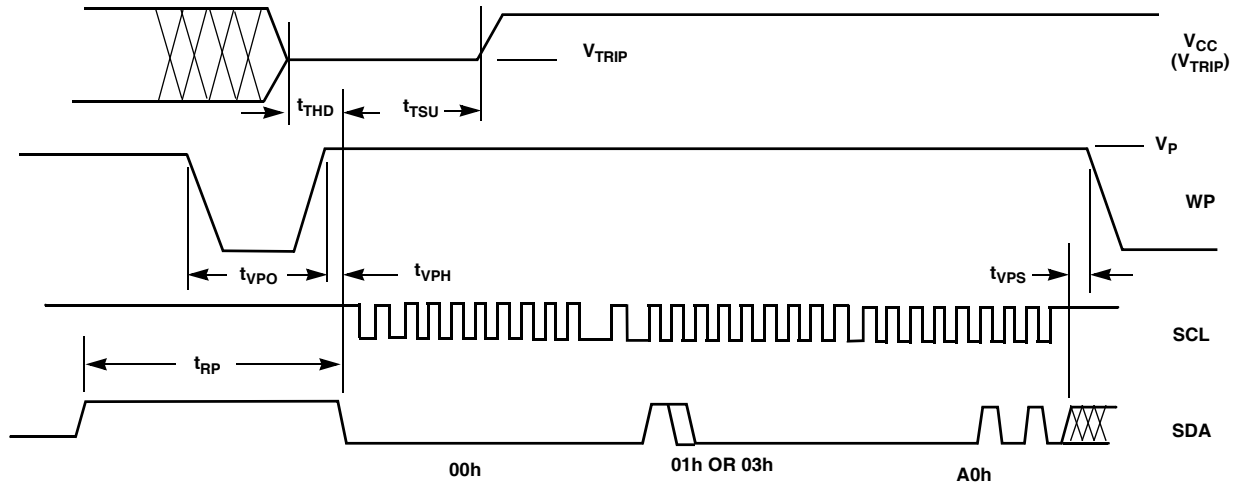


## VTRIP Programming Parameters

| PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{VPS}$ | $V_{TRIP}$ Program Enable Voltage Set-up Time | 1 | | µs |
| $t_{VPH}$ | $V_{TRIP}$ Program Enable Voltage Hold Time | 1 | | µs |
| $t_{TSU}$ | $V_{TRIP}$ Set-up Time | 1 | | µs |
| $t_{THD}$ | $V_{TRIP}$ Hold (Stable) Time | 10 | | ms |
| $t_{WC}$ | $V_{TRIP}$ Write Cycle Time | | 10 | ms |
| $t_{VPO}$ | $V_{TRIP}$ Program Enable Voltage Off Time (Between Successive Adjustments) | 0 | | µs |
| $t_{RP}$ | $V_{TRIP}$ Program Recovery Period (Between Successive Adjustments) | 10 | | ms |
| $V_P$ | Programming Voltage | 15 | 18 | V |
| $V_{TRAN}$ | $V_{TRIP}$ Programmed Voltage Range | 1.7 | 5.0 | V |
| $V_{ta1}$ | Initial $V_{TRIP}$ Program Voltage Accuracy ($V_{CC}$ Applied - $V_{TRIP}$) (Programmed At +25°C.) | -0.1 | +0.4 | V |
| $V_{ta2}$ | Subsequent $V_{TRIP}$ Program Voltage Accuracy [($V_{CC}$ Applied - $V_{ta1}$) - $V_{TRIP}$ programmed at +25°C.] | -25 | +25 | mV |
| $V_{tr}$ | $V_{TRIP}$ Program Voltage Repeatability (Successive Program Operations. Programmed at +25°C.) | -25 | +25 | mV |
| $V_{tv}$ | $V_{TRIP}$ Program Variation After Programming (0°C to +75°C). (Programmed at +25°C) | -25 | +25 | mV |

## *Mini Small Outline Plastic Packages (MSOP)*



INDEX AREA

**TOP VIEW**

0.20 (0.008) | A | B | C

**SIDE VIEW**

0.10 (0.004) | C
0.20 (0.008) | C

GAUGE PLANE

SEATING PLANE

SEATING PLANE

0.25 (0.010)

4X θ

4X θ

**END VIEW**

0.20 (0.008) | C | D
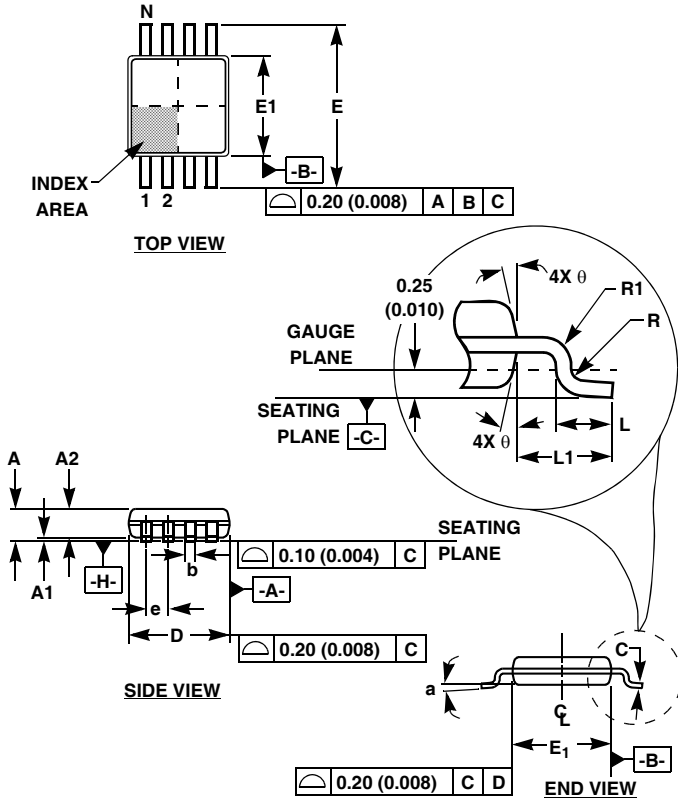
### M8.118 (JEDEC MO-187AA)
**8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|--------|--------|-------------|--------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.037 | 0.043 | 0.94 | 1.10 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 | - |
| b | 0.010 | 0.014 | 0.25 | 0.36 | 9 |
| c | 0.004 | 0.008 | 0.09 | 0.20 | - |
| D | 0.116 | 0.120 | 2.95 | 3.05 | 3 |
| E1 | 0.116 | 0.120 | 2.95 | 3.05 | 4 |
| e | 0.026 BSC | | 0.65 BSC | | - |
| E | 0.187 | 0.199 | 4.75 | 5.05 | - |
| L | 0.016 | 0.028 | 0.40 | 0.70 | 6 |
| L1 | 0.037 REF | | 0.95 REF | | - |
| N | 8 | | 8 | | 7 |
| R | 0.003 | - | 0.07 | - | - |
| R1 | 0.003 | - | 0.07 | - | - |
| 0 | 5º | 15º | 5º | 15º | - |
| α | 0º | 6º | 0º | 6º | - |

Rev. 2 01/03

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.

2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

3. Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. -H- Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.

5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).

10. Datums -A- and -B- to be determined at Datum plane -H-.

11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

For information regarding Intersil Corporation and its products, see www.intersil.com

## *Small Outline Package Family (SO)*
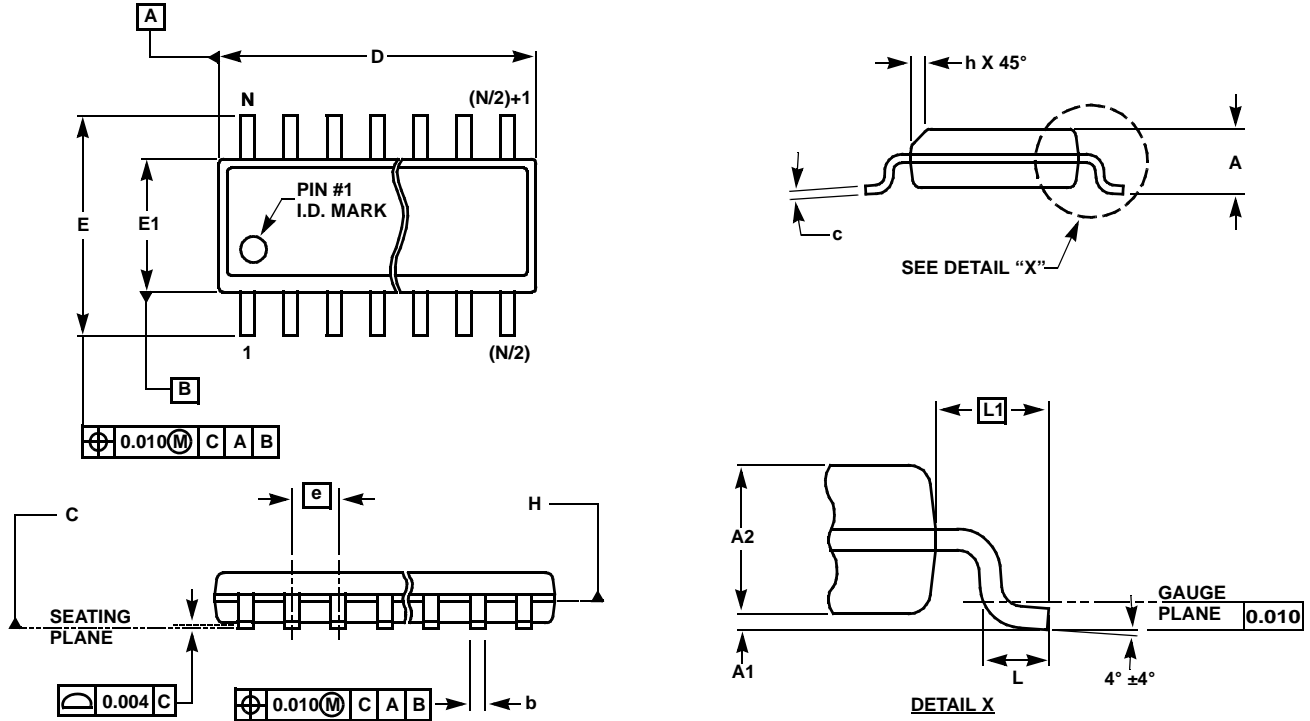


## MDP0027

**SMALL OUTLINE PACKAGE FAMILY (SO)**

| SYMBOL | SO-8 | SO-14 | SO16 (0.150") | SO16 (0.300") (SOL-16) | SO20 (SOL-20) | SO24 (SOL-24) | SO28 (SOL-28) | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | | | INCHES | | | | | |
| A | 0.068 | 0.068 | 0.068 | 0.104 | 0.104 | 0.104 | 0.104 | MAX | - |
| A1 | 0.006 | 0.006 | 0.006 | 0.007 | 0.007 | 0.007 | 0.007 | ±0.003 | - |
| A2 | 0.057 | 0.057 | 0.057 | 0.092 | 0.092 | 0.092 | 0.092 | ±0.002 | - |
| b | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | ±0.003 | - |
| c | 0.009 | 0.009 | 0.009 | 0.011 | 0.011 | 0.011 | 0.011 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | 0.406 | 0.504 | 0.606 | 0.704 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | 0.406 | 0.406 | 0.406 | 0.406 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | 0.295 | 0.295 | 0.295 | 0.295 | ±0.004 | 2, 3 |
| e | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | 0.030 | 0.030 | 0.030 | 0.030 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | 0.056 | 0.056 | 0.056 | 0.056 | Basic | - |
| h | 0.013 | 0.013 | 0.013 | 0.020 | 0.020 | 0.020 | 0.020 | Reference | - |
| N | 8 | 14 | 16 | 16 | 20 | 24 | 28 | Reference | - |

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994